**Amendments To The Specification**

Please insert the following two new paragraphs after existing paragraph [0012]

[0012.1] Fig. 7E illustrates a cross-sectional view of the partial semiconductor device of Fig. 7D, with the addition of a dummy structure and a via.

[0012.2] Fig. 7F illustrates a cross-sectional view of a partial semiconductor device according to an embodiment of the present disclosure.

Please replace paragraph [0026] with the following amended paragraph:

[0026] Referring now to Fig. 7D, shown therein is another cross-sectional view of a partial semiconductor device according to one embodiment of the present disclosure. In this embodiment, a top dielectric layer 90 may be deposited by plasma enhanced chemical vapor deposition (PE-CVD) techniques. The layer 90 may have a thickness of approximately 2000 to 8000 Angstroms. Vias may then be formed in the dielectric layers 86 and 88, and another metallurgy level and dielectric layer may be formed according to procedures known in the art. More specifically, Fig. 7E is a cross-sectional view that is the same as Fig. 7D, except that a dummy structure 92 of another metallurgy level is shown diagrammatically in broken lines on the dielectric layer 90, and a via is shown diagrammatically in broken lines at 94, the via extending between and thermally coupling the dummy structures 42 and 92. In addition, Fig. 7F is a cross-sectional view of a partial semiconductor device according to an embodiment of the present disclosure, the left and right halves of Fig. 7F each being effectively identical to Fig. 7E. Thus, Fig. 7F shows two dummy structures 42 in one metallurgy level and two dummy structures 92 in a different metallurgy level, each dummy structure 42 being thermally coupled to a respective one of the dummy structures 92 by a respective via 94.